

1 **What is claimed is:**

1 1. A method of forming a dual-layer resist, comprising
2 the steps of:

3 providing a substrate;
4 forming a patterned first resist layer on the substrate;
5 curing the first resist layer so that the first resist
6 layer does not dissolve in a resist solvent; and
7 forming a patterned second resist layer on the cured
8 first resist layer.

1 2. The method as claimed in claim 1, wherein the step
2 of curing the first resist layer is performed by ion
3 implantation of argon or nitrogen into the first resist
4 layer.

1 3. The method as claimed in claim 2, wherein the ion
2 implantation is performed using an energy of 10 to 50 keV and
3 a dose of 10^{13} to 10^{15} ions/cm².

1 4. The method as claimed in claim 1, wherein the step of
2 curing the first resist layer is performed using argon
3 plasma.

1 5. A method of coding a mask read only memory,
2 comprising the steps of:

3 providing a substrate having thereon a mask read only
4 memory array consisted of a plurality of memory
5 cells;
6 forming a first resist layer having repetitive patterns
7 to shield a partial area of each memory cell and
8 expose the places for ion implantation;

9 curing the first resist layer so that the first resist
10 layer does not dissolve in a resist solvent;
11 forming a patterned second resist layer on the cured
12 first resist layer to shield a partial area of the
13 mask read only memory array; and
14 performing code implantation to change the logic state
15 of the memory cell not shielded by the second
16 resist layer.

1 6. The method as claimed in claim 5, wherein the first
2 resist layer shields a plurality of bit lines in the mask
3 read only memory array, wherein each bit line is composed of
4 a semiconductor doped area.

1 7. The method as claimed in claim 5, wherein the step
2 of curing the first resist layer is performed by ion
3 implantation of argon or nitrogen into the first resist
4 layer.

1 8. The method as claimed in claim 5, wherein the ion
2 implantation is performed using an energy of 10 to 50 keV and
3 a dose of 10^{13} to 10^{15} ions/cm².

1 9. The method as claimed in claim 5, wherein the step
2 of curing the first resist layer is performed using argon
3 plasma.

1 10. A method of forming holes, comprising the steps of:
2 providing a substrate having a dielectric layer thereon;
3 forming a first resist layer having substantially
4 parallel first trench patterns on the dielectric
5 layer;

6 curing the first resist layer so that the first resist
7 layer does not dissolve in a resist solvent;
8 forming a second resist layer having substantially
9 parallel second trench patterns on the cured first
10 resist layer, wherein the second trench patterns
11 are substantially perpendicular to the first
12 trench patterns; and
13 removing the dielectric layer under the intersections of
14 the second trench patterns and the first trench
15 patterns to form at least one hole.

1 11. The method as claimed in claim 10, wherein the step
2 of curing the first resist layer is performed by ion
3 implantation of argon or nitrogen into the first resist
4 layer.

1 12. The method as claimed in claim 11, wherein the ion
2 implantation is performed using an energy of 10 to 50 keV and
3 a dose of 10^{13} to 10^{15} ions/cm².

1 13. The method as claimed in claim 10, wherein the step
2 of curing the first resist layer is performed using argon
3 plasma.

1 14. The method as claimed in claim 10, wherein the
2 dielectric layer is mainly silicon dioxide.

1 15. A method of manufacturing a dual damascene
2 structure, comprising the steps of:
3 providing a substrate having a dielectric layer thereon;
4 forming a first resist layer having a plurality of hole
5 patterns on the dielectric layer;

6 curing the first resist layer so that the first resist
7 layer does not dissolve in a resist solvent;
8 forming a second resist layer having a plurality of
9 second trench patterns on the cured first resist
10 layer;
11 etching the dielectric layer using the first resist
12 layer as a mask to transfer the hole patterns to
13 the dielectric layer; and
14 etching the first resist layer and the dielectric layer
15 using the second resist layer as a mask to
16 transfer the trench patterns to the dielectric
17 layer.

1 16. The method as claimed in claim 15, wherein the two
2 steps of transferring the hole patterns and transferring the
3 trench patterns are performed by a same processing
4 instrument.

1 17. The method as claimed in claim 15, wherein the step
2 of curing the first resist layer is performed using ion
3 implantation of nitrogen into the first resist layer.

1 18. The method as claimed in claim 17, wherein the ion
2 implantation is performed using an energy of 10 to 50 keV and
3 a dose of 10^{13} to 10^{15} ions/cm².

1 19. The method as claimed in claim 15, wherein the step
2 of curing the first resist layer is performed using argon
3 plasma.

1 20. The method as claimed in claim 15, wherein the
2 dielectric layer is mainly silicon dioxide.